ABSTRACT OF THE DISCLOSURE

An integrated semiconductor memory having selection transistors can be formed at a web. The web can be arranged on an insulation layer. The first source/drain region can be arranged on the insulation layer at one lateral end of the web and the second source/drain region can be arranged on the insulation layer at another lateral end of the web. The longitudinal sides of the web and a top side of the web can be covered with a layer sequence including a gate dielectric and a gate electrode. High write-read currents can be achieved in the on state of the selection transistors and leakage currents occurring in the off state can be reduced.